

**Remarks**

Applicant respectfully requests reconsideration of the rejection of the claims in view of the claim amendments above and the remarks set forth below. Claims 1-20 remain in the application. Claims 1-4, 7, 9-11, 13-16, 18-20 are amended. Claims 5, 6, 8, 12 and 17 were previously presented.

**35 U.S.C. §103**

Claims 1 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dejonghe et al. (US 6,636,084) in view of Park et al. (US 6,470,030) in further view of Nakai et al. (US 6,247,034). In order to support a prima facie case of obviousness under 35 U.S.C. § 103(a), each and every element of the claim must be shown in the references cited. The applicants respectfully propose neither Dejonghe, Park, nor Nakai, taken individually or in combination show all of the elements of the amended claim 1.

Amended independent claim 1 recites, inter alia, an "Orthogonal Frequency Division Multiplexing (OFDM) receiver . . . comprising . . . a shared buffer that stores data corresponding to the OFDM signals . . . a processor that is adapted to receive data from the shared buffer, perform computations on the data and return data to the shared buffer . . . an equalizer module adapted to receive data from the shared buffer and equalize the data . . . and a receiver controller that controls access to the shared buffer by the processor and controls the transfer of data from the shared buffer to the equalizer module." Support for the amendment can be found, among other places, on page 10, lines 1-15 and in FIG. 3. No new matter is added.

The "shared buffer that stores data corresponding to the OFDM signals" is an important element of the claimed invention. More specifically, the "shared buffer" element overcomes the shortcomings of the conventional buffer arrangement of using a separate buffer associated with each functional block. The conventional buffer arrangement and shortcomings are described as follows on page 3, lines 1-5 of the application:

The functional blocks or modules of OFDM receivers are typically connected in series so that the output of one functional block goes into a buffer associated with the next functional block. This arrangement takes up space and increases the processing overhead associated with processing OFDM signals. A buffer architecture that avoids these shortcomings would be desirable.

In other words, the “shared buffer” element of amended claim 1 overcomes the shortcoming of the conventional buffer arrangement used in OFDM receivers since a plurality of separate buffers between functional blocks is not used. Rather, one “shared buffer” is used by all of the functional blocks.

Dejonghe appears to be directed at an OFDM receiver containing a storing unit connected in series between a complex multiplier and a frequency offset acquisition unit (FIG. 4; Col. 7, lns. 6-10). Dejonghe appears to merely describe the conventional buffer arrangement discussed above, i.e., connecting a buffer in series between two processing blocks.

Park appears to be directed towards an OFDM receiver having a rearrangement memory connected in series between an FFT processor and a synchronizing section (FIG. 1; Col. 3, lns. 44-56). As a result, similarly to Dejonghe, Park appears to merely describe the conventional arrangement of connecting a buffer in series between two processing blocks.

Nakai appears to be directed towards an FFT processing unit containing a single processing element, a butterfly operation unit, connected to two RAM memory units under control by a controller unit (FIG. 1; Col. 8, ln. 30 to col. 9, ln. 27). The RAM memory units are dedicated for the operation of the butterfly operation unit. Nakai does not appear to show or suggest that the RAM memory units are shared with additional processing elements.

In contrast to Dejonghe, Park and Nakai, amended claim 1 recites “a shared buffer that stores data corresponding to the OFDM signals...a processor that is adapted to receive data from the shared buffer, perform computations on the data and return data to the shared buffer...an equalizer module adapted to receive data from the shared buffer and equalize the data... and a receiver controller that controls access to the shared buffer by the processor and

controls the transfer of data from the shared buffer to the equalizer module.” Neither Dejonghe, Park, nor Nakai, individually or in combination, show or suggest the “shared buffer” element of amended claim 1. Indeed, Dejonghe, Park and Naka appear to merely illustrate the conventional buffering arrangement discussed in the background of the application (page 3, Ins. 1-5). As discussed above, the claimed “shared buffer” element of amended claim 1 overcomes the shortcomings of the conventional buffering arrangement. As a result, it is respectfully proposed that the rejection for obviousness under 35 U.S.C. § 103(a) is overcome and notice to that effect is earnestly solicited.

Dependent claims 2-12 being dependent on and further limiting independent claim 1, should be allowable for that reason, as well as for the additional recitations that they contain. Applicant respectfully requests reconsideration of the rejection of the claims in view of the above amendments and remarks.

Independent claim 13 is amended to contain elements similar to amended independent claim 1 and should be allowable for the reasons discussed above. Therefore, it is respectfully proposed that the rejection for obviousness is overcome.

Dependent claims 14-20 being dependent on and further limiting amended independent claim 13, should be allowable for that reason, as well as for the additional recitations that they contain. Applicant respectfully requests reconsideration of the rejection of the claims in view of the above remarks.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the Applicants' attorney at (818) 260-3727, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fees, other than those discussed above, are believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,



By: Vincent E. Duffy

Reg. No. 39,964

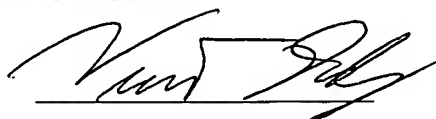
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Patent Operations  
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June 27, 2008

#### CERTIFICATE OF MAILING

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

6/27/08  
date

  
Vincent E. Duffy

Report to Data Base  
 Docket No. P0200354  
 Inventor(s): Maxim Borisovich Belotserkovsky, et al.  
 Title: Certified Buffer Architecture For an OFDM Receiver

PATENT OPERATIONS  
 Serial No. 10/523,442 Filed: 1/31/05  
 Patent No. \_\_\_\_\_  
 Atty: Vincent E. Duffy

MAILING TO U.S. Patent and Trademark Office

APPLICATION AS FILED

Enter Date	Enter Number	Check Type	Check Items Mailed with Application	Express Mail Application Label No.:
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		Claims in Excess 20	<input type="checkbox"/> Divisional	
		Claim Pages	<input type="checkbox"/> Continuation	
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			REQUESTS	
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